CLAIMS

Please amend the claims as follows and enter new claims 19-23 for consideration.

1. (Currently amended) A system for transmitting from a current stage having a host system to a next stage with limited clock jitter, a signal containing either digital video from a preceding stage or digital video from the host system of the current stage, comprising:

a digital video scaler (DVS) for ~~scaling~~reclocking the digital video received from the preceding stage to a constant ~~resolution~~frequency;

a constant-frequency clock connected to the DVS; and

a multiplexer for selecting either the ~~scaled~~reclocked digital video from the DVS or the digital video from the host system of the current stage.

2. (Currently amended) The system of claim 1, wherein said DVS comprises:

a retiming FIFO for retiming the ~~received~~digital video received from the preceding stage; and

a scaling engine for scaling the retimed digital video ~~data~~ to match [[the]]a constant resolution.

3. (Original) The system of claim 1, further comprising a receiver for receiving a signal containing digital video from the preceding stage.

4. (Previously presented) The system of claim 1, wherein said signal is a Transition Minimized Differential Signaling (TMDS) signal.

5. (Previously presented) The system of claim 1, wherein said signal is a Low-Voltage Differential Signaling (LVDS) signal.

6. (Original) The system of claim 1, wherein said signal contains audio.

7. (Currently amended) A method of transmitting from a current stage having a host system to a next stage with limited clock jitter, a signal containing either digital video from a preceding stage or digital video from the host system of the current stage, comprising the steps of:

~~scaling~~reclocking the digital video received from the preceding stage to a constant ~~resolution~~frequency using a constant-frequency clock; and

selecting between the ~~scaled~~reclocked digital video and the digital video from host system of the current stage.

8. (Currently amended) The method of claim 7, wherein said step of ~~scaling~~reclocking comprises the steps of:

retiming the digital video received from the preceding stage; and

creating video data matching [[the]]a constant resolution from the retimed video data.

9. (Currently amended) The method of claim 7, wherein said step of ~~scaling~~reclocking further comprises the step of superimposing an on-screen display (OSD) message.

10. (Previously presented) The method of claim 7, wherein the signal is a Transition Minimized Differential Signaling (TMDS) signal.

11. (Previously presented) The method of claim 7, wherein the signal is a Low-Voltage Differential Signaling (LVDS) signal.

12. (Original) The method of claim 7, wherein the signal contains audio.

13. (Previously presented) A method of transmitting from a current stage having a host system to a next stage with limited clock jitter, a signal containing either digital video from a preceding stage or digital video from the host system of the-current stage, comprising the steps of:

selecting between the digital video from the preceding stage and the digital video from the current stage; and

~~scaling~~reclocking the selected digital video to a constant ~~resolution~~frequency using a constant-frequency clock wherein the digital video is also reclocked at the previous stage and the next stage.

14. (Original) The method of claim 13, wherein said step of ~~scaling~~reclocking the selected digital video comprises the steps of:

retiming the selected digital video using a FIFO; and

creating video data matching to the constant resolution from the retimed data.

15. (Previously presented) The method of claim 13, wherein the signal is a Transition Minimized Differential Signaling (TMDS) signal.

16. (Previously presented) The method of claim 13, wherein the signal is a Low-Voltage Differential Signaling (LVDS) signal.

17. (Currently amended) A system for transmitting, from a current stage having a host system to a next stage with limited clock jitter, a signal containing either digital video from a preceding stage or digital video from the host system of the current stage, comprising:

a multiplexer for selecting either received digital video from the preceding stage or the video from the host system of the current stage;

a digital video scaler (DVS) for ~~scaling~~reclocking the digital video received from the multiplexer to a constant ~~resolution~~frequency; and

a constant-frequency clock connected to the DVS.

18. (Previously presented) The system of claim 17, wherein said DVS comprises:

a retiming FIFO for retiming the received video from the multiplexer, and a scaling engine for scaling the retimed video data to a constant resolution.

19. (New) The system of claim 1, wherein a single DVS is also contained in the preceding stage, the next stage and subsequent stages such that the video signal is reclocked by the DVS at each stage.

20. (New) The method of claim 7, wherein the digital video is reclocked at the preceding stage, the next stage and subsequent stages.

21. (New) The method of claim 13, wherein the selected digital video is relocked at the preceding stage, the next stage and subsequent stages.

22. (New) The system of claim 17, wherein a single DVS is also contained in the preceding stage, the next stage and subsequent stages such that the video signal is reclocked by the DVS at each stage.

23. (New) A digital video scaler for reducing jitter in a video signal comprising:

a jitter-reducing retiming FIFO buffer having a clock input receptive to a video signal; and

a scaling engine having a scaling engine input coupled to said retiming FIFO buffer whereby said retiming FIFO buffer and said scaling engine are clocked by a common clock.